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Finite-Difference Time-Domain Analysis of Flip-Chip Interconnects with Staggered Bumps

Hussein H. M. Ghouz and El-Badawy El-Sharawy

***Abstract*— This paper presents finite-difference time-domain (FDTD) analysis of flip-chip interconnects. Transition between coplanar waveguides on the chip and the mother board are investigated over a broad band of frequency by means of Fourier transform of the time-domain results. Objectives of the analysis include the evaluation of bump reflection and insertion loss as well as the reconfiguration of the transition to improve package performance. Novel designs have been developed and presented to reduce the effects of package discontinuities and asymmetry. Staggering the bumps has been found to reduce reflection and insertion loss over a broad band of frequency. A reduction in bump reflection of up to 8 dB per transition can be achieved by staggering the ground and signal connects. The degradation in package performance due to structure asymmetry is also studied. The present designs have been also found to reduce the effects of flip-chip asymmetry on insertion and reflection losses.**

I. Introduction

Coplanar waveguide structures (CPW's) are important planar transmission lines in microwave and millimeter-wave integrated circuits. Analysis of CPW lines has been performed using the finite-difference time-domain (FDTD) method to predict pulse response of the line [1]–[5]. Such a transmission line offers several advantages over the conventional microstrip for monolithic and hybrid microwave integrated circuits (MMIC) applications [5]. These advantages include the ease of parallel and series insertion of both active and passive components and high circuit density. Using CPW in MMIC eliminates the need for the costly back process which includes thinning the substrate, via hole etching and metallization. Typically, 30% of GaAs chips are lost in this process alone.

The popularity of CPW in MMIC applications resulted in increased interest in flip chip packaging due to the compatibility between flip-chip applications and CPW circuits. Flip chip is emerging as the lead technology in multichip module packages [6]–[9]. Several chips can be mounted together to a mother board using flip chip to increase density, improve system performance and reduce cost. This packaging technique also allows combinations of active and passive devices, silicon and gallium arsenide, and probably analog and digital circuits in the same application. In fact, transitions in flip chip coplanar waveguide structure involve the use of metallic bumps to transmit the signal between the chip and the package. The geometry and design of the bumps constitute the basics of flip chip interconnects. These bumps represent a discontinuity to the signal propagating on the line which results in partial loss, reflection and possibly distortion of the signal. In addition, due to misalignment between the mother board and the chip and possible unequal degradation of solder connects, asymmetry of the lumps may result. This can occur, in particular, when large bumps (2 mils or more) are used to align very small bumps (half a mil or less) [10]. As a result, the conventional CPW mode (the odd mode) may couple to undesired modes (the even mode) [11].

This work is mainly concerned with the FDTD analysis and evaluation of frequency dependent parameters of the transition between two coplanar waveguides on two separate substrates connected via metallic bumps. The objectives of the present model is to investigate

Manuscript received June 11, 1995; revised February 15, 1996.
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Publisher Item Identifier S 0018-9480(96)03795-7

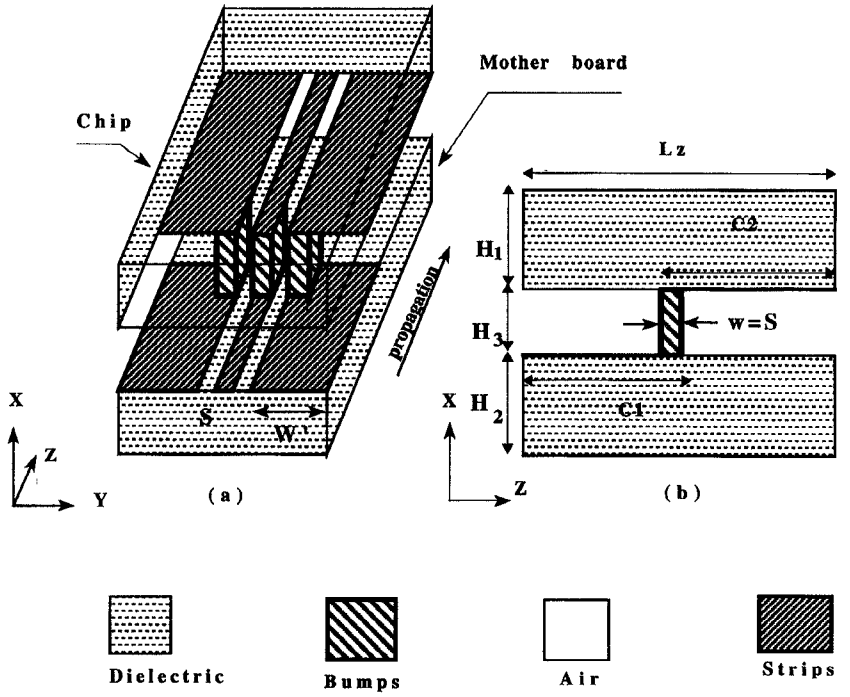

Fig. 1. Flip chip CPW with open termination (basic configuration). (a) Three-dimensional view. (b) Side view. $H_1 = H_2 = 0.36$ mm, $H_3 = 0.12$ mm, $S = W = 0.12$ mm, $W' = 0.6$ mm, $C_1 = 3.12$ mm, $C_2 = 2.16$ mm, $L_z = 5.04$ mm.

new designs of flip chip CPW structures which minimize the bump reflection and insertion loss over a broad frequency band. Fig. 1 illustrates the basic configuration of the flip chip CPW structure. This is referred to as flip chip CPW structure with open termination.

Section II of this paper presents a brief discussion of FDTD method used for analysis and modeling. This includes the excitation source requirements and boundary condition treatment. Frequency dependent parameters are also discussed in this section. Results of return loss and insertion loss of the flip chip transitions are presented in Section III, and the paper is concluded Section IV.

II. Finite-Difference Time-Domain Method

In our analysis, we assume that media under consideration are uniform, isotropic, homogeneous and has no magnetic properties, i.e., $\mu_r \cong 1$. Furthermore, we assume that ground and center conductors are perfect conductors (PEC) and have zero thickness. A Gaussian pulse is used to modulate the transverse spatial distribution of the excitation fields as

$$E_x(x, y) = \psi_x(x, y) \cdot \exp\left[\frac{-(t-t_o)^2}{T^2}\right] \tag{1}$$

$$E_y(x, y) = \psi_y(x, y) \cdot \exp\left[\frac{-(t-t_o)^2}{T^2}\right] \tag{2}$$

where

$\psi_x(x, y)$ The spatial distribution function for x-component of the electric field.

$\psi_y(x, y)$ The spatial distribution function for y-component of the electric field.

t_o Time center of the pulse.

T Pulse width.

The spatial distribution functions, $\psi_x(x, y)$ and $\psi_y(x, y)$, are not initially known. However, a quasistatic TEM mode assumption can be used as initial guess. In this work, a quasistatic distribution is launched in a CPW structure with the same dielectric layers as the flip chip structure. The length of this CPW will be assumed as the reference in our calculations and is chosen such that the mode will be developed at the output. This output is then used as the correct spatial distribution functions $\psi_x(x, y)$ and $\psi_y(x, y)$ for all flip chip structures in our simulation.

To simulate infinite structures, absorbing boundary conditions (ABC's) have to be added at the six outer walls of the computational domain. There are different techniques for simulating an ABC. In our simulation, we use the first-order Mur absorbing boundary conditions due to its simplicity and stability [13]. At the source plane, we apply the excitation field components (E_x and E_y) until the pulse is completely lunched, and then, switch to the ABC to avoid reflection from the source plane. Another boundary treatment is the air-dielectric interface where, the average dielectric constant is used, i.e., $(\varepsilon_1 + \varepsilon_2)/2$. Furthermore, in our simulation a technique of nonuniform mesh is used to reduce the memory requirement as well as to improve the accuracy of the results [4].

The performance of the flip-chip interconnect can be characterized by evaluating the frequency-dependent parameters. These are insertion loss and return loss, and given by

$$IL(\omega) = \left[\frac{P_{out}(z_{out}, \omega)}{P^f_{in}(z_{in}, \omega)}\right] \tag{3}$$

$$RL(\omega) = \left[\frac{P_r(z_{in}, \omega)}{P^f_{in}(z_{in}, \omega)}\right] \tag{4}$$

where

$P_{out}(z_{out}, \omega)$ Denotes the power at the output line of the flip chip CPW structure.

$P_r(z_{in}, \omega)$ Denotes the power reflected due to the bump discontinuity.

$P^f_{in}(z_{in}, \omega)$ Denotes the power at the input port of the reference CPW structure.

III. Results

In a flip chip CPW package, bumps represent the main discontinuity and their effects may overlap with other types of discontinuities including dielectric and impedance discontinuities. In dielectric dis-

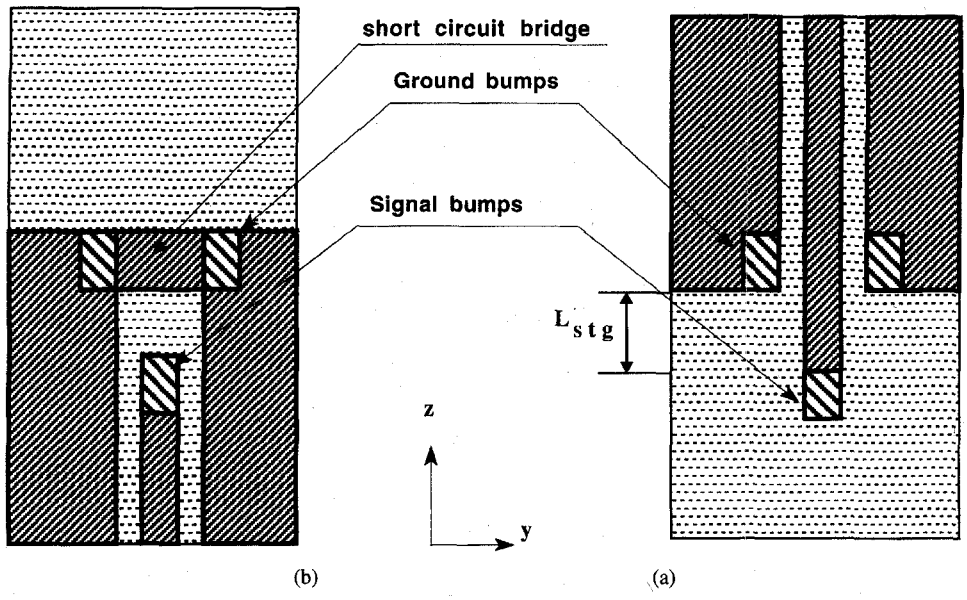

Fig. 2. Flip chip CPW-CPW with staggered bumps and short circuit bridge. (a) Top view of cpw-chip. (b) Top view of cpw-mother board.

continuity, the material dielectric constant and dimensions of the chip and the mother boards are different, even though the characteristic impedance of lines on the two substrates may be the same. Impedance discontinuity occurs when the lines on the two substrates have different characteristic impedance. To isolate the effects of bump discontinuity, we assumed that both chip and mother board have the same dielectric constants and thickness and the CPW lines are identical on both substrates.

We have verified our code by calculating the s-parameters of a transition between a CPW and a microstrip line through a via hole and comparing the results to those of [12]. Excellent agreement has been observed between our work and the above reference. Further verification of our code was carried out by calculating the effective dielectric constant and the characteristic impedance of a multilayer CPW structure using both the method of moment and the FDTD method. Here, the effective dielectric constant is defined as $(\beta^2/\omega^2\mu_o\varepsilon_o)$. Excellent agreement has been obtained between the effective dielectric constants computed using the two methods as shown in Fig. 3. The computed characteristic impedance using either the moment method or the FDTD was approximately 50 ohms and varied very slightly over the entire band. Again, the difference between the two methods was negligible (less than 2%). In the following results the multilayer CPW structure will be used as a reference for calculating the insertion and return losses.

Fig. 4 shows the return and insertion losses due to the bump structure of Fig. 1. As frequency increases, losses increase. The figure also shows the return and insertion losses of a staggered configuration. Staggering the bumps has been found to reduce the reflection and insertion loss for frequencies up to 50 GHz. The reduction in reflection loss is about 8 dB at 50 GHz. This is due to the fact that reflection from ground and signal bumps do not add in phase which leads to less reflection. At high frequencies, staggering the bumps may, however, increase insertion loss due to possible resonance when reflections are out of phase. The frequency at which staggering the bumps starts to result in adverse effects on insertion and return losses depends on the dimensions of the CPW and the bumps. A parametric study of the flip chip structure indicates that there are optimum dimensions at which insertion and return losses are minimum. As shown in Fig. 4, a staggering distance L_{stg} of two slot width gave the minimum insertion and return loss. The losses have been also studied versus bump dimensions. In general, decreasing the

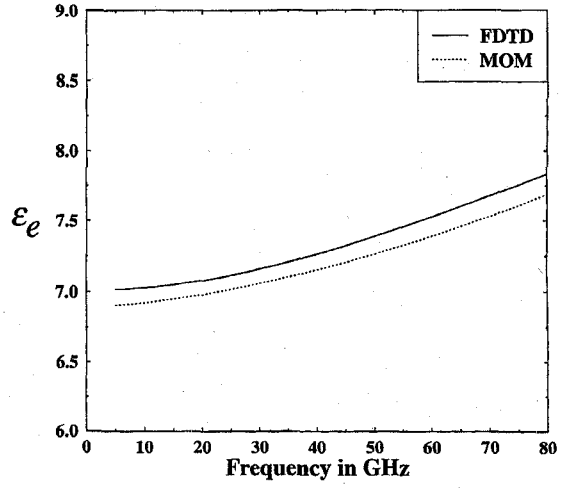

Fig. 3. Effective dielectric constant of reference CPW.

bump height or the cross section reduces losses. However, bump cross section is limited by the conductor width of CPW and the minimum height is determined by the fabrication process.

Staggering the signal and ground bumps will reduce coupling due to the increased distance between these bumps as compared to the in-line bumps (referred to in Fig. 1 as the open end structure). The low coupling in the staggered case can reduce the effects of the asymmetry of the ground bumps on the center bump current which may result in overall reduction of the effects of asymmetry on the package performance. (The current density on the center bump is approximately twice the current density on the two ground bumps.) We have studied the effects of flip chip asymmetry on the performance of CPW transitions by reducing the cross section of one the ground bumps. Referring to Fig. 5, one of the ground bump cross sections is reduced by approximately 33% and is simulated for three configurations including a short circuit bridge between the ground bumps. This short tends to equalize the potential of the two ground sides of a CPW and therefore reduce the effects of asymmetry [5]. The asymmetry increased reflection and insertion losses. The effects of staggering the bumps and adding a short circuit bridge at the discontinuity are evident in reducing the reflection and insertion loss for frequencies up to 50 GHz. We tested other cases of asymmetry

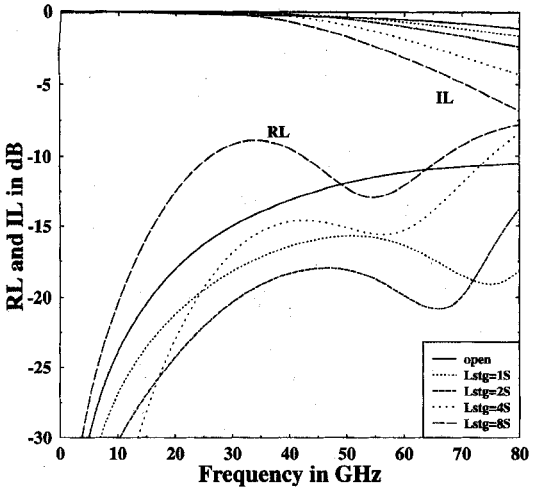

Fig. 4. Return loss and insertion loss of symmetric flip chip CPW with staggered bumps.

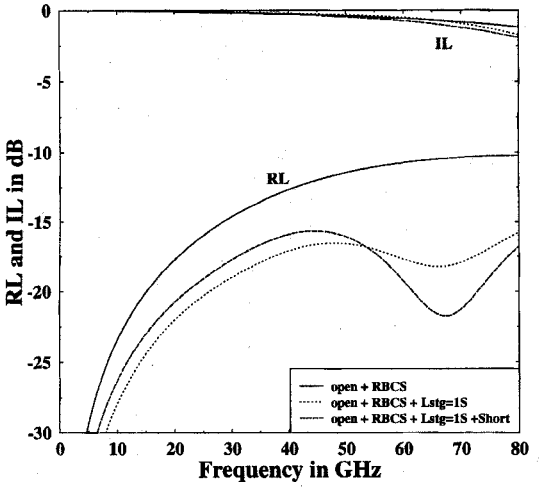

Fig. 5. Return loss and insertion loss of asymmetric flip chip CPW with staggered bumps and short circuit bridge.

including removing one of the ground bumps, or misplacing one of the bumps. In all these cases, the staggered configurations performed better than the in-line bump configurations.

IV. Conclusion

A three-dimensional (3-D) FDTD computer code have been developed to model and investigate the transition between two coplanar waveguides on the chip and the mother board over a wide frequency range. Our results includes three different CPW transitions. These are open, staggered and short circuit bridge. Using these models, we investigated the effects of the bump discontinuity and the structure asymmetry on the performance of a flip chip CPW package. The results indicate that a reduction of the bump reflection can be obtained using the staggered bumps and the short circuit bridge designs. A reduction in the bump reflection of up to 8 dB is achieved over a wide frequency range. However, the insertion loss improvement may not be very significant. The effect of structure asymmetry has been studied. The deterioration of the package performance due to asymmetry can be significantly reduced by incorporating one of the above designs.

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Thermal Management for High-Power Active Amplifier Arrays

Nicholas J. Kolias and Richard C. Compton

***Abstract*—Much of the active array work reported to date has been directed toward the demonstration of prototypes at low-power levels. Analysis results presented here show that overheating failures will occur as these arrays are scaled to reasonable output powers. Large air-cooled heat sinks attached to the backside of a thinned array can be used for single-sided designs such as oscillator arrays, but heat sinking becomes substantially more difficult for two-sided transmission-type arrays. For these designs, a possible solution is described which uses an aluminum-nitride dielectric layer to facilitate conduction to heat sinks on the array's perimeter.**

I. Introduction

Quasi-optical active arrays provide a means of combining the outputs of large number of semiconductor devices [1]–[8]. Such arrays could provide an alternative to tubes for high power millimeter

Manuscript received June 11, 1995; revised February 15, 1996. This work was supported by the Army Research Office.

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Publisher Item Identifier S 0018-9480(96)03794-5.